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(54) Gray scale processing for a display device, using error diffusion

(57) In an error diffusion processing unit one dot of input signal is converted into plural picture elements. The respective picture elements (pixels) thus converted are compared with prior data to detect the luminance error, which will then be weighted by multiplying it with certain coefficients to give, for instance, the reproduced vertical error, horizontal error and diagonal error which will respectively be added to the original pixels. Producing a false tone by error diffusion in units of pixel enables to display the half tone without reducing the spatial resolution.

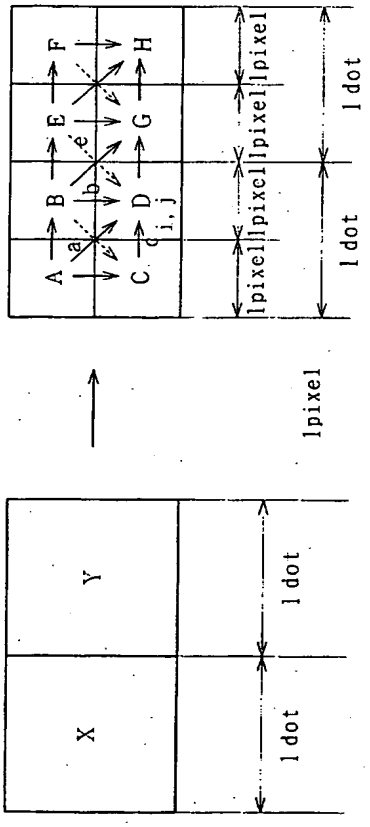

Fig.6

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Description

This invention relates to the display driving method and drive that can have a high density and fine image by constituting one dot of input signal with plural picture elements and displaying the half tone by way of error variance in unit of pixel.

Recently PDP (Plasma Display has been attracting a great deal of public attention as a thin, light-weighted display device. Totally different from the conventional CRT drive system, the drive method of this PDP is a direct drive by means of digitalized image input signal. Consequently, the luminance and tone of the light emitted from the panel face depends on the bit number of the signal to be processed.

PDP may be divided into two types: AC and DC types whose basic characteristics are different from each other. The DC drive type PDP has reportedly improved the luminance and service life which had been one of the longstanding questions. This type of PDP is therefore progressing toward its commercial use.

AC type features satisfactory characteristics as far as is concerned the luminance and durability. As for the tonal display, maximum 64 tones only have reportedly been displayed at the level of trial production.

It is however proposed to adopt in future a technique for 256 tones by address/display separate type drive method (ADS subfield method).

FIGURES 1(a) and (b) are the drive sequence and drive waveform of the PDP used in this method.

In FIGURE 1(a), one frame consists of 8 subfields whose relative ratios of luminance are 1, 2, 4, 8, 16, 32, 64 and 128 respectively. Combination of these 8 luminances enables a display in 256 tones. The respective subfields are composed of the address duration that writes in one screen of refreshed data and the sustaining duration that decide the luminance level of the corresponding fields. In the address duration, first wall charge is formed initially at each pixel simultaneously over all the screens for display. The brightness of the subfield is proportional to the number of the sustaining pulse to be set to predetermined luminance. Two hundred and fifty-six tones display is thus realized.

Since said address duration is constant irrespectively of the length of the sustaining duration, the more the number of tones in such an AC drive method, the more the number of bits of the address duration is as the preparation time for lighting up and making the panel luminescent within one frame of duration increases. The sustaining duration as light emitting duration becomes thus relatively short thereby reducing the maximum luminance.

Because the luminance and tone of the light emitted from the panel face depends upon the number of bits of the signal to be processed, increased number of the bits of the signal improves the picture quality, but decreases the emission luminance. If conversely the number of the bits of the signal to be processed is decreased, the emission luminance increases but it decreases the tone to be displayed, causing thus the degradation of the picture quality.

The error variance intended to minimize the color depth difference between the input signal and emission luminance rendering the number of the bits of the output drive signal smaller than that of the input signal, is a process to express false tone used when the maximal shade of color is desired to be manifested with lesser tone.

FIGURE 2 shows a conventional, general variance circuit, where an image signal with the original picture elements or pixels Ai, j of n (8, for example) bits is input into an image signal input terminal 30. This image signal is processed in a vertical adder 31 and horizontal adder 32, its bit number being reduced to m (4, for example). After passing through an image output terminal 34 and PDP drive circuit, it makes the PDP luminescent.

On the other hand, the error variance signal from the foregoing horizontal adder 32 is compared with the data just before which has been stored in ROM 38 of the error detect circuit 35. If there is any difference between these signals, the adder 39 gives the sum thereof and weights it by multiplying it with coefficient at the level of the error weight circuits 40 and 41 to get an error detect output. This error detect output is added to the vertical adder 31 through the intermediary of the h-line delay circuit 36 that outputs the reproduced error Ej-1 generated in the 1-line past and at the same time, added to the horizontal adder 32 through the intermediary of the d-dot delay circuit 37 that outputs the reproduced error Ei-1 that was generated in the past before d dots than the original picture element Ai,j, for example, 1 dot before. The coefficients at the level of the error weight circuits 40 and 41 are to be so set that the sum total of these coefficients should be one (1).

As a result, a corrected luminance line as y=x (dotted line) is obtained despite the instantaneous emission luminance in steplike form (solid line) to be expressed in 4 bits, which in fact is recognized as smoothed-out shape because the emission luminance levels above and below said steps (solid line) are output alternately according to a given proportion.

The driving method as shown in FIGURE 1(a) adopts 256 tones dividing one frame into 8 subfields. Increasing this number of tones reduces the emission luminance. If, conversely, the bit number of the signal to be processed is decreased composing one frame with 6 subfields as shown in FIGURE 3(a), the emission luminance increases. If the same is done configuring one frame with 4 subfields as shown in FIGURE 3(b), the increasing trend of emission luminance becomes greater.

Such half tone display technique as has been described was problematical in that it reduces the resolution and elicits particular patterns because the brightness is diffused in the respective directions of vertical, horizontal and time.

The purpose of this invention is to provide such a driving method and drive that do not allow reduced resolution and elicitation of particular patterns even if the number of bits is reduced of the signal to be processed.

In order to achieve the objective, this invention converts, at the pixel/dot conversion part 50, one dot into 4 pictures: A, B, C, and D. One of the elements, for instance, D is assumed to have entered into the error variance circuit 28.

The picture element D, when entering the error detect circuit 35 within the error variance circuit 28, is compared with the data A, B, and C just before that have been previously stored in ROM 38. The sum thereof is given by the adder 39 and it is then weighted by multiplying it with the respective coefficients at the error weight circuit 40, 41 and 53 to obtain the error signals b, c, and a respectively. The reproduced error b past by one line, for instance, is added to the vertical adder 31 through the intermediary of the h-line delay circuit 36. The reproduced error c past by one dot is added to the horizontal adder 32 through the intermediary of the d-dot delay circuit 37. Further, the reproduced error a, past by 1 line and 1 dot is added to the picture element D at the diagonal adder 51 through the intermediary of the p-line, q-dot delay circuit.

Producing the half tone by error variance in unit of pixel with respective reproduced errors a, b, and c added up allows to display the half tone without expanding the half tone display area beyond the required number of dots (resolution).

Consequently this invention has the effect that the resolution does not decrease and particular patterns do not appear even if the number of bits is reduced of the signal to be processed.

A particular embodiment in accordance with this invention will now be described with reference to the accompanying drawings, in which:-

FIGURE 1 represents the drive sequence and drive waveform in the 256-tone technique;

FIGURE 2 is a block diagram that shows a conventional display drive;

In FIGURE 3, (a) illustrates the drive sequence in 64-tone technicity and, (b) the drive sequence in 32-tone one;

FIGURE 4 gives the characteristic line of drive signal vs. emission luminance level in a conventional circuit;

FIGURE 5 is a block diagram that depicts an embodiment of the display drive by this invention;

FIGURE 6 is an explicative diagram that illustrates the actions of the half tone display by pixel conversion and error variance processing according to this invention; and

FIGURE 7 is another explicative diagram showing plural embodiments of the picture element conversion.

The basic way of thinking in this invention is as follows.

The reduced resolution in the conventional half tone technique was caused by the variance area of half tone which is wider than the required number of dots (resolution).

This inconvenience cannot be dissolved theoretically as far as the display driving method implying "required number of dots= number of picture elements" is adopted.

Note that actually the display device is becoming ever larger, and with this the largeness of one dot is becoming larger and larger. For instance, the size of one dot for 21-inch type PDP is 0.66 mm × 0.66 mm, and that for 42-inch PDP is 0.8mm × 0.8mm.

This invention is characterized in that such display configuration as "required number of dots < number of picture elements" has been realized by displaying one dot by plural pixels to produce the half tone with error variance by units of pixels in one dot.

If the half tone is produced and displayed by means of the error variance in unit of pixel within one dot, the half tone can be displayed without extending the half tone display area beyond the required number of dots (resolution).

On the drive circuit side, therefore, the half tone display technique with the required number of dots ensured under the conditions of reduced number of bits and increased emission luminance, enables to have a fine image with higher luminance.

Referring now in particular to the drawings, there are illustrated the embodiments of this invention. The invention will be understood more readily with reference to the display device constituting one dot with four pixels; however these examples are intended to illustrate the invention and are not to be construed to limit the scope of this invention.

In FIGURE 5, the numeral 30 represents an image signal input terminal with n bits of original pixels, to which an image of required number of bits is transferred. The required dots may be, for instance, horizontal 640 × vertical 480 dots, equivalent to VGA.

This image signal input terminal 30 is connected to the pixel/dot conversion part 50 that converts one dot into plural, for example, 4 pixels, and further to the PDP as display panel through the error variance circuit 28 and the drive part 43, which may or may not include such a bit conversion circuit 33 as shown in FIGURE 2 intended to reduce the number of bits of the output drive signal rather than that of the input signal.

The error variance circuit 28 consists of a vertical adder 31, a horizontal adder 32, a diagonal adder 51, an error detect circuit 35, an h-line delay circuit 36, a d-dot delay delay circuit 37, and p-line/q-dot delay circuit 52.

The error detect circuit 35 comprises the ROM 38 that stores the past data, the adder 39 that adds the data of this ROM 38 to the data as input, the error weighting

circuits 40, 41 and 53 that weight the added output by multiplying it with the predetermined coefficient to output the reproduced error generated between the error detect output and the picture elements prior to the original pixels.

The driving part 43 can use lower number of display tones so that the driving is made for respective pixels, if one dot of the image input signal is composed of the half tone output equally divided both vertically and horizontally into four pixels.

In the foregoing configuration, one dot of the image signal of the original pixel as input into the image signal input terminal 30 is converted into plural pixels at the pixel/dot conversion part 50.

The plural pixels undergo the error variance processing in pixel unit by the error variance circuit 28 to display the half tone.

We now assume that the respective single dots of the image signals X and Y of the original pixels input as shown in FIGURE 6 are converted into 4 pixels of A, B, C, and D on the one hand, and into E, F, G, and H on the other, respectively at the pixel/dot conversion part 50.

The invention is now described referring to the case of the error variance of the picture element D (i, j). The pixel /dot conversion part 50 converts one dot into 4 pixels with the pixel D entering into the error variance circuit 28.

When the pixel D inputs into the error detect circuit 35by way of the vertical adder 31, horizontal adder 32 and diagonal adder 51, it is compared with the data A, B, and C stored in the ROM 38 to detect a positive or negative error, the adder 39 sums up the error and the input data, and the error weighting circuits 40, 41 and 53 weight the sum by multiplying this sum with their respective coefficients to get the error signals b, c, and a respectively. These error detect signals b, c, and a, that is the reproduced error b generated before 1 line, for instance, is added to pixel D at the vertical adder 31 through the h-line delay circuit 36, the reproduced error c generated before 1 dot is added to the same by the horizontal adder 32 through the d-dot delay circuit 37, and finally the reproduced error a generated before 1 line and 1 dot is added to the same by the diagonal adder 51 through the p-line q-dot delay circuit 52.

Generally, the coefficients at the error weighting circuits 40, 41, and 53 are to be set in such a way that the total sum of them should be one (1).

When the respective reproduced errors a, b, a and c are added up and sent to the driving part 43, this par 43, using lower number of display tone, drives the respective pixel units to display the half tone.

Thus producing the half tone performing the error variance for pixel unit within 1 dot, allows to display the half tone without extending the half tone display area beyond the required number of dots (resolution).

In the foregoing embodiment the error variance has been done for pixel D by combining the reproduced errors a, b, and c. However it is not limited by this combination. It will also do by such combinations as a only, b only, c only, combinations of a and b, a and c, and b and c. Further it may be added e.

Also in the foregoing embodiment one dot of image input signal has been equally divided, as half tone output both vertically and horizontally, into 4 pixels as shown in FIGURE 7(a), but the invention is not limited to this type of embodiment. One dot of image input signal may be divided, as half tone output, equally divided vertically and trisected horizontally into six pixels as shown in FIGURE 7(b), or else one dot of image input output, only horizontally into three pixels as shown in FIGURE 7(c).

Thus the number of divisions is all optional both vertically and horizontally.

In the foregoing embodiment, the image signal of the original picture elements input into the image signal input terminal 30, may reduce the number of bits of the signal to be processed by configuring one frame with 6 subfields as shown in FIGURE 3(a), or with 4 subfields as shown in FIGURE 3(b), all having such steplike luminance levels with larger level differences than in FIGURE 4.

Claims

1. A display driving method characterized in that in an error variance processing circuit that gets a false half tone diffusing in the surroundings the luminance error between the image signal of original picture elements quantizedly input and the preceding data, one dot of said image signal of the original pixels is composed of plural pixels to display the half tone exercising the error variance based on the data of past pixels by this one unit of pixel.

2. A display drive characterized in that in an error variance processing circuit that gets a false half tone diffusing in the surroundings the luminance error between the image signal of original picture elements quantizedly input and the preceding data, the drive comprises the pixel/dot conversion part (50) that converts one dot of the original pixel image signal into plural pixels, the error variance circuit (28) that outputs reproduced error for every pixel based on the input data and the data stored beforehand to add the output of the reproduced error for every pixel of the input signal and finally the driving part (43) with lower number of display tones intended to display the half tone with respective pixels which have undergone the error variance.

3. The display drive as claimed in Claim 2, wherein the pixel/dot conversion part (50) converts one dot into four pixels and the error variance circuit (28) comprises the error detect circuit (35) that outputs, for every pixel, any one or more reproduced error in at

least one of vertical, horizontal and diagonal directions based on the input data and the data stored beforehand, a delay circuit that delays the reproduced error, and finally an adder that ads the output of the delay circuit for every original pixel as input.

4. The display drive as claimed in Claim 3, wherein the error detect circuit (35) comprises the memory (38) that stores the past data beforehand, the adder (39) that adds the data from the memory (38) to the data as input, and the error weighting circuit that weights the added output by predetermined coefficients to output the reproduced error generated between the error detect output and the pixel prior to the original picture element.

5. The display drive as claimed in Claim 2, 3 or 4, wherein the display panel comprises PDP or liquid crystal display panel.

Fig. 1

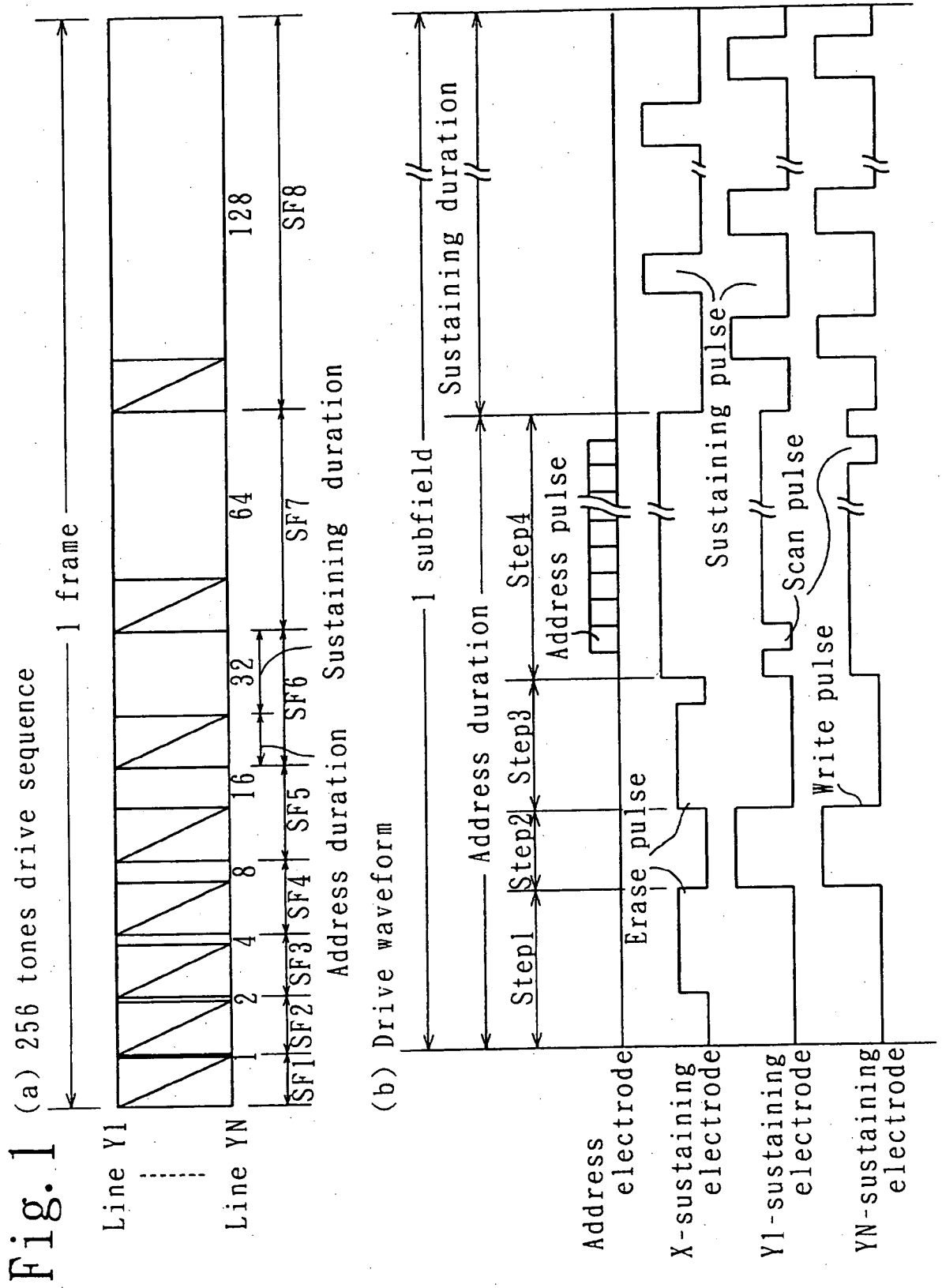

(a) 256 tones drive sequence
1 frame
Line Y1
Line YN
1
2
4
8
16
32
64
128
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
Address duration
Sustaining duration
(b) Drive waveform
1 subfield
Sustaining duration
Address duration
Step1
Step2
Step3
Step4
Address pulse
Erase pulse
Sustaining pulse
Scan pulse
Write pulse
Address electrode
X-sustaining electrode
Y1-sustaining electrode
YN-sustaining electrode

Fig. 2

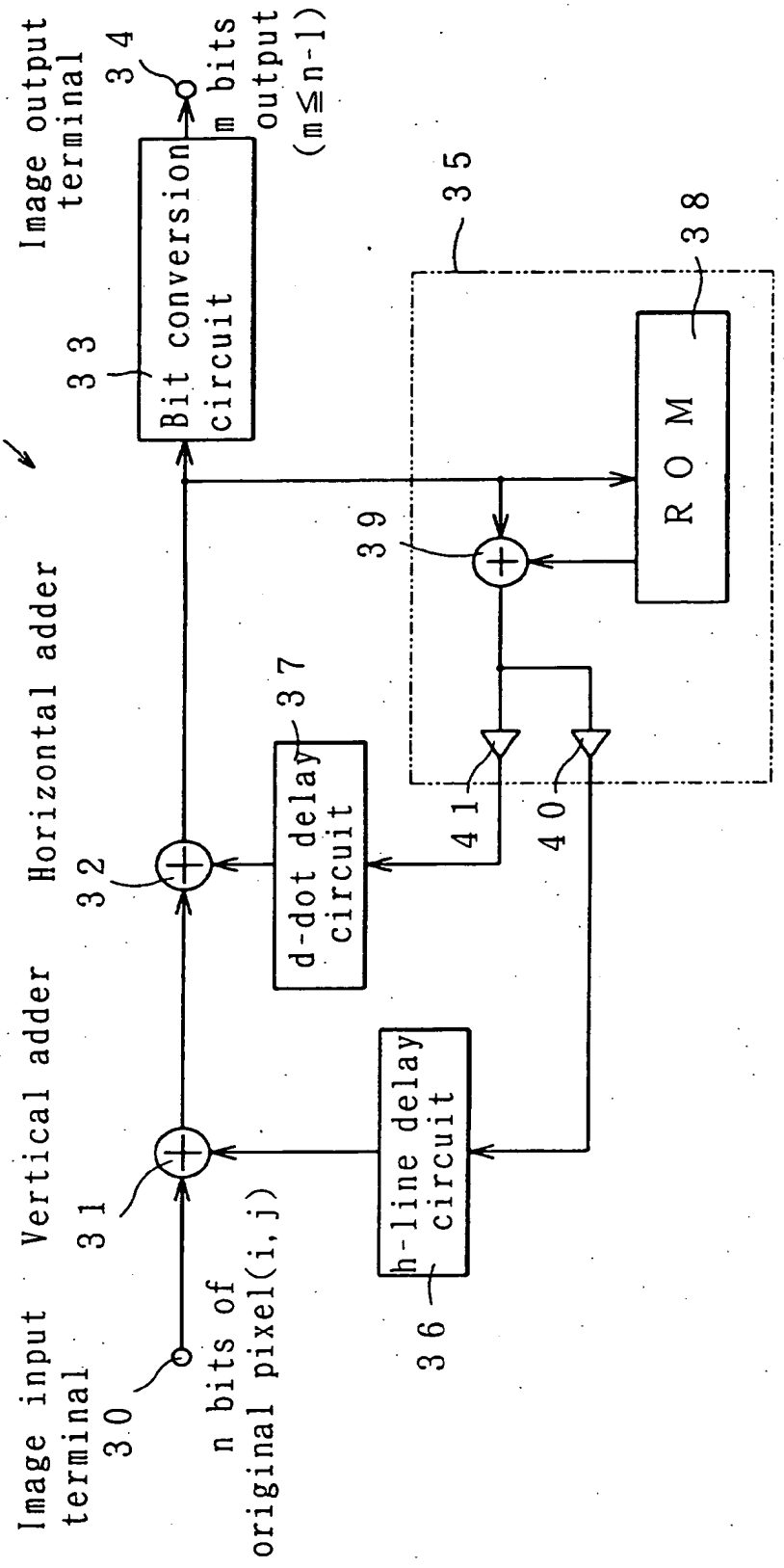


Fig. 3

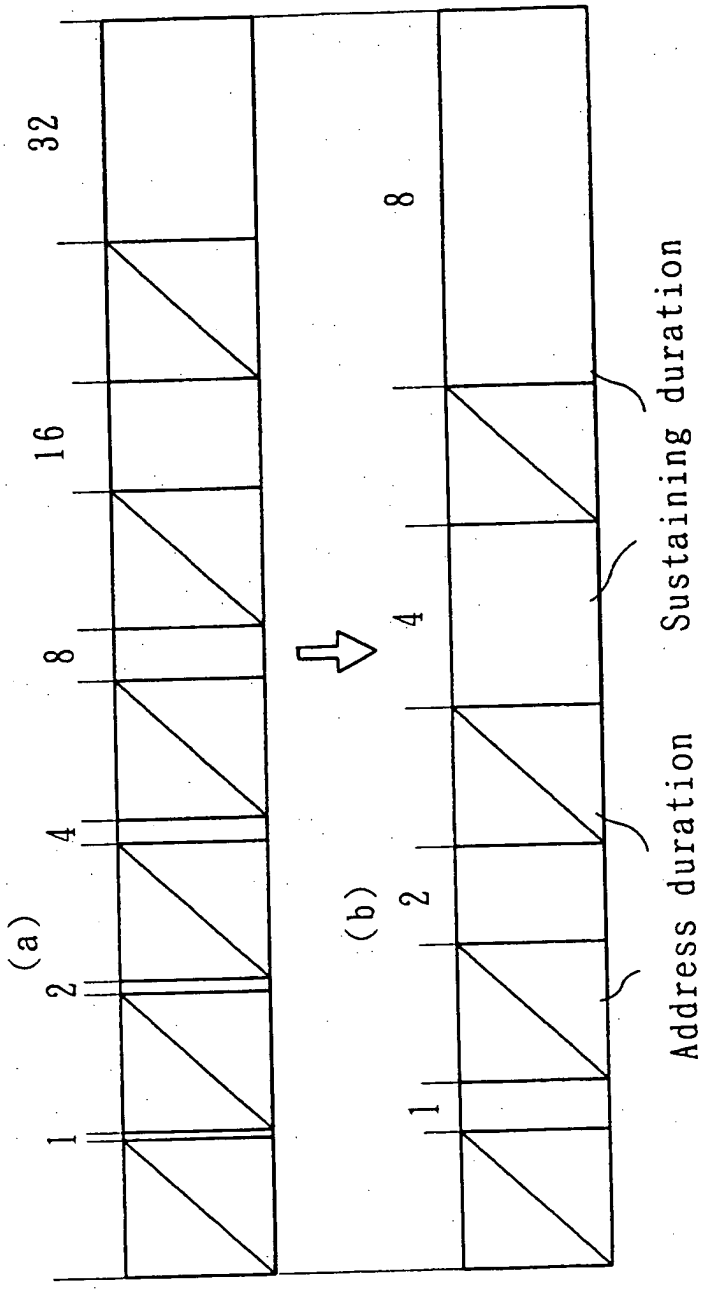


Fig. 4

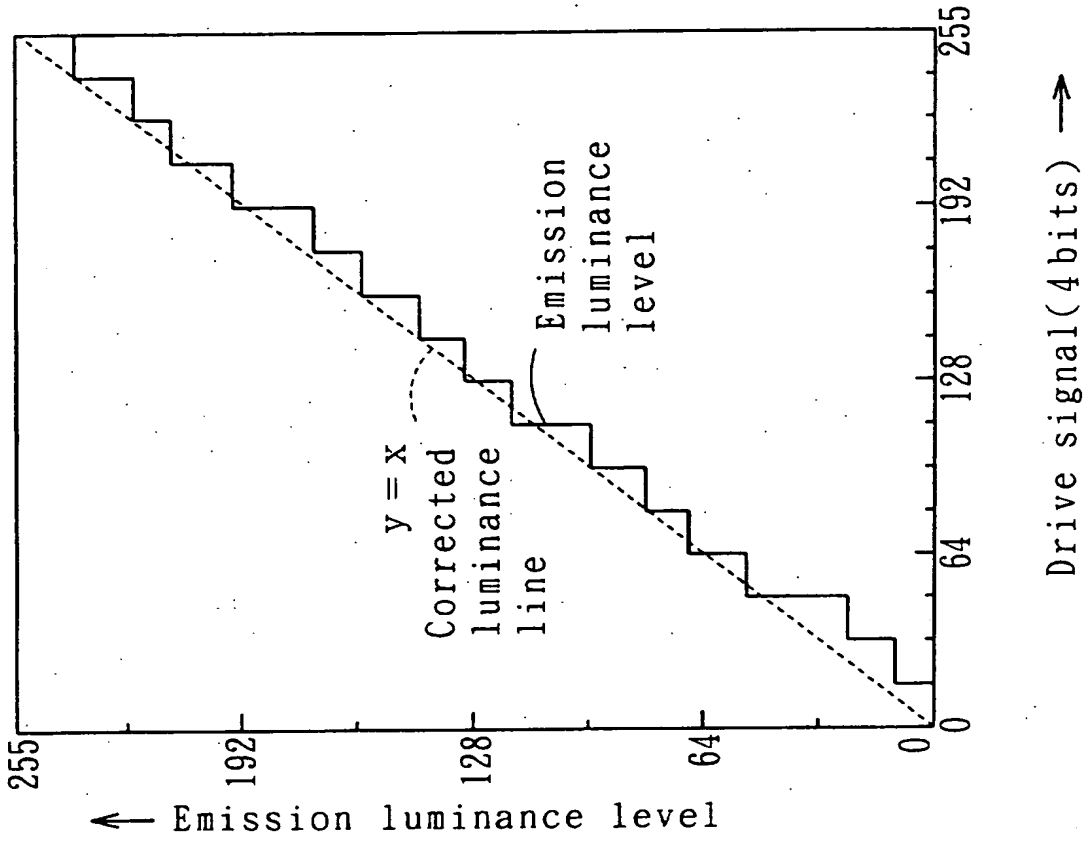


Fig. 5

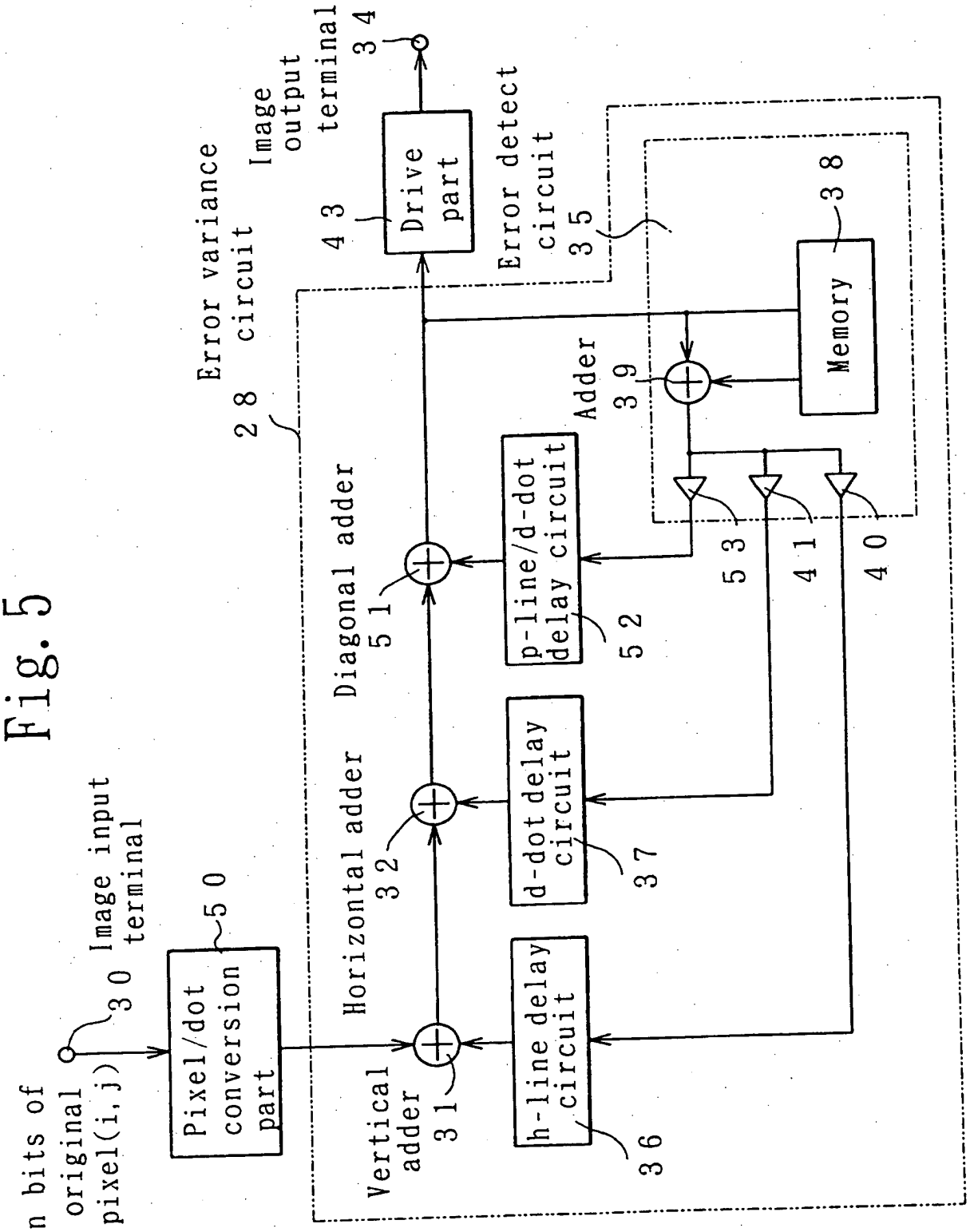


Fig. 6

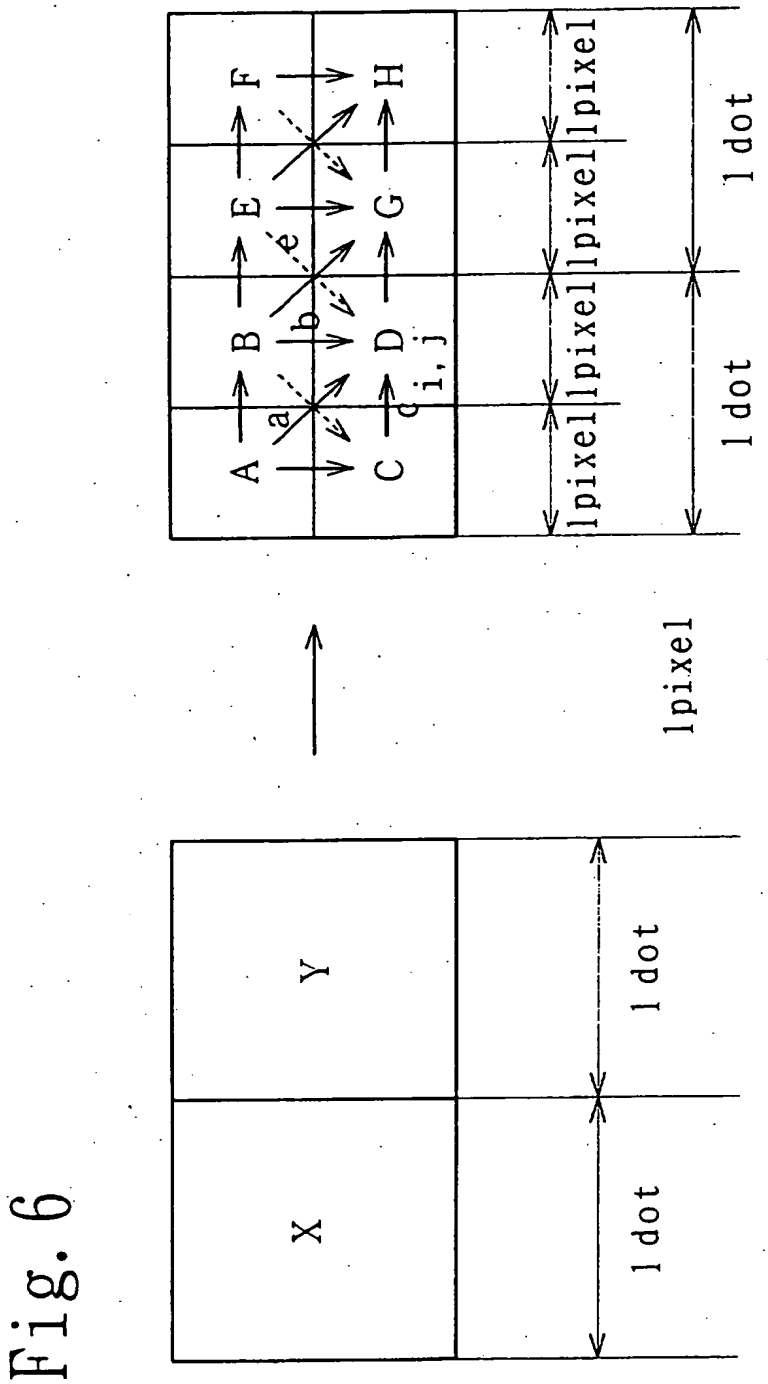
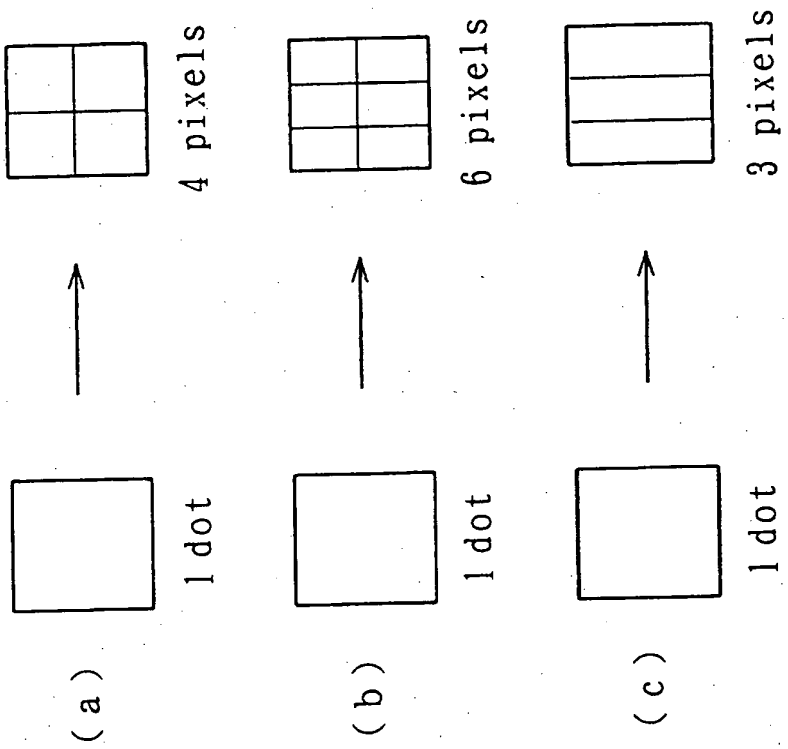


Fig. 7



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EUROPEAN SEARCH REPORT

Application Number
EP 95 30 8188

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 264 302 (MATSUSHITA ELECTRIC INDUSTRIAL CO.) * column 1, line 1 - column 2, line 5 * * figure 1 *	1-5	G09G3/28 G09G3/20
A	SID INTERNATIONAL SYSMPOSIUM, DIGEST OF TECHNICAL PAPERS, May 1992 PLAYA DEL REY, CA. USA, pages 713-716, XP 000479110 KANAGU ET AL. 'A 31 inch-diagonal full-color surface-discharge ac plasma display panel' * page 715, left column, line 1 - right column, line 11 * * figure 3 *	1-4	
A	GB-A-2 202 661 (COMPAQ COMPUTER CO.) * page 12, line 23 - page 13, line 7 *	1,2	
A	EP-A-0 579 359 (CANON K.K.)		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G09G
H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 March 1996	Farricella, L

CATEGORY OF CITED DOCUMENTS

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